

Low Noise, Low Drift FET Op Amp

AD645

FEATURES

Improved Replacement for Burr-Brown OPA-111 and OPA-121 Op Amp

LOW NOISE
- 2 μV p-p max, 0.1 Hz to 10 Hz
- 10 nV/√Hz max at 10 kHz
- 11 fA p-p Current Noise 0.1 Hz to 10 Hz

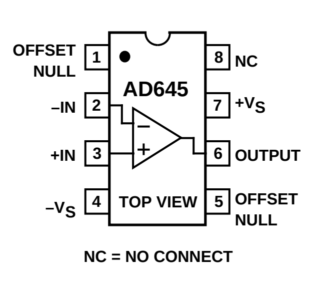
HIGH DC ACCURACY
- 250 μV max Offset Voltage
- 1 μV/°C max Drift
- 1.5 pA max Input Bias Current
- 114 dB Open-Loop Gain
- Available in Plastic Mini-DIP, 8-Pin Header Packages, or Chip Form

IMPROVED DRIFT

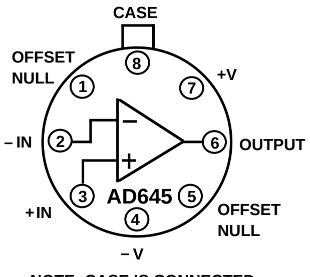
APPLICATIONS
- Low Noise Photodiode Preamps
- CT Scanners
- Precision I-V Converters

CONNECTION DIAGRAMS

8-Pin Plastic Mini-DIP (N) Package



TO-99 (H) Package



The AD645 is available in six performance grades. The AD645J and AD645K are rated over the commercial temperature range of 0°C to +70°C. The AD645A, AD645B, and the ultra-precision AD645C are rated over the industrial temperature range of –40°C to +85°C. The AD645S is rated over the military temperature range of –55°C to +125°C and is available processed to MIL-STD-883B.

The AD645 is available in an 8-pin plastic mini-DIP, 8-pin header, or in die form.

PRODUCT DESCRIPTION

The AD645 is a low noise, precision FET input op amp. It offers the pico amp level input currents of a FET input device coupled with offset drift and input voltage noise comparable to a high performance bipolar input amplifier.

The AD645 has been improved to offer the lowest offset drift in a FET op amp, 1 μV/°C. Offset voltage drift is measured and trimmed at wafer level for the lowest cost possible. An inherently low noise architecture and advanced manufacturing techniques result in a device with a guaranteed low input voltage noise of 2 μV p-p, 0.1 Hz to 10 Hz. This level of dc performance along with low input currents make the AD645 an excellent choice for high impedance applications where stability is of prime concern.

PRODUCT HIGHLIGHTS

1. Guaranteed and tested low frequency noise of 2 μV p-p max and 20 nV/√Hz at 100 Hz makes the AD645C ideal for low noise applications where a FET input op amp is needed.
2. Low V_{OS} drift of 1 μV/°C max makes the AD645C an excellent choice for applications requiring ultimate stability.
3. Low input bias current and current noise (11 fA p-p 0.1 Hz to 10 Hz) allow the AD645 to be used as a high precision preamp for current output sensors such as photodiodes, or as a buffer for high source impedance voltage output sensors.

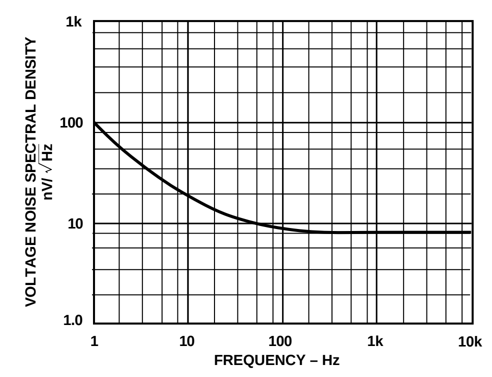


Figure 1. AD645 Voltage Noise Spectral Density vs. Frequency

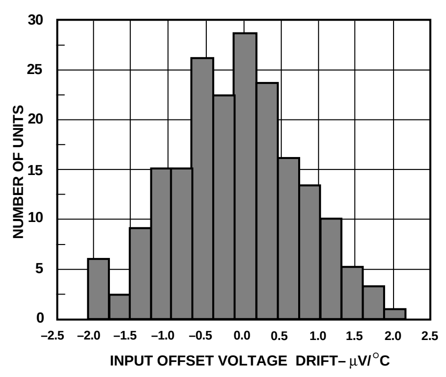


Figure 2. Typical Distribution of Average Input Offset Voltage Drift (196 Units)

REV. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703

AD645–SPECIFICATIONS (@ +25°C, and ±15 V dc, unless otherwise noted)

Model	Conditions[1]	AD645J/A			AD645K/B			AD645C			AD645S			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
INPUT OFFSET VOLTAGE[1]														
Initial Offset			100	500		50	250		50	250		100	500	µV
Offset	T_{MIN}–T_{MAX}		300	1000		100	400		75	300		500	1500	µV
Drift (Average)			3	10/5		1	5/2		0.5	1		4	10	µV/°C
vs. Supply (PSRR)		90	110		94	110		94	110		90	110		dB
vs. Supply	T_{MIN}–T_{MAX}		100		90	100		90	100		86	95		dB
INPUT BIAS CURRENT[2]														
Either Input	V_{CM} = 0 V		0.7/1.8	3/5		0.7/1.8	1.5/3		1.8	3		1.8	5	pA
Either Input @ T_{MAX}	V_{CM} = 0 V		16/115			16/115			115			1800		pA
Either Input	V_{CM} = +10 V		0.8/1.9			0.8/1.9			1.9			1.9		pA
Offset Current	V_{CM} = 0 V		0.1	1.0		0.1	0.5		0.1	0.5		0.1	1.0	pA
Offset Current @ T_{MAX}	V_{CM} = 0 V		2/6			2/6			6			100		pA
INPUT VOLTAGE NOISE	0.1 to 10 Hz		1.0	3.0		1.0	2.5		1	2		1.0	3.3	µV p-p
	f = 10 Hz		20	50		20	40		20	40		20	50	nV/√Hz
	f = 100 Hz		10	**30**		10	**20**		10	**20**		10	**30**	nV/√Hz
	f = 1 kHz		9	15		9	12		9	12		9	15	nV/√Hz
	f = 10 kHz		8	10		8	10		8	10		8	10	nV/√Hz
INPUT CURRENT NOISE	f = 0.1 to 10 Hz		11	20		11	15		11	15		11	20	fA p-p
	f = 0.1 thru 20 kHz		0.6	1.1		0.6	0.8		0.6	0.8		0.6	1.1	fA/√Hz
FREQUENCY RESPONSE														
Unity Gain, Small Signal			2			2			2			2		MHz
Full Power Response	V_O = 20 V p-p R_{LOAD} = 2 kΩ	16	32		16	32		16	32		16	32		kHz
Slew Rate, Unity Gain	V_{OUT} = 20 V p-p R_{LOAD} = 2 kΩ	1	2		1	2		1	2		1	2		V/µs
SETTLING TIME[3]														
To 0.1%			6			6			6			6		µs
To 0.01%			8			8			8			8		µs
Overload Recovery[4]	50% Overdrive		5			5			5			5		µs
Total Harmonic Distortion	f = 1 kHz R_{LOAD} ≥ 2 kΩ V_O = 3 V rms		0.0006			0.0006			0.0006			0.0006		%
INPUT IMPEDANCE														
Differential	V_{DIFF} = ±1 V		10^{12}‖1			10^{12}‖1			10^{12}‖1			10^{12}‖1		Ω‖pF
Common-Mode			10^{14}‖2.2			10^{14}‖2.2			10^{14}‖2.2			10^{14}‖2.2		Ω‖pF
INPUT VOLTAGE RANGE														
Differential[5]			±20			±20			±20			±20		V
Common-Mode Voltage		±10	+11, –10.4		±10	+11, –10.4		±10	+11, –10.4		±10	+11, –10.4		V
Over Max Oper. Range		±10			±10			±10			±10			V
Common-Mode Rejection Ratio	V_{CM} = ±10 V	90	110		94	110		94	110		90	110		dB
	T_{MIN}–T_{MAX}		100		90	100		90	100		86	100		dB
OPEN-LOOP GAIN	V_O = ±10 V R_{LOAD} ≥ 2 kΩ	114	130		120	130		120	130		114	130		dB
	T_{MIN}–T_{MAX}				114			114			110			dB
OUTPUT CHARACTERISTICS														
Voltage	R_{LOAD} ≥ 2 kΩ	±10	±11		±10	±11		±10	±11		±10	±11		V
	T_{MIN}–T_{MAX}	±10			±10			±10			±10			V
Current	V_{OUT} = ±10 V	±5	±10		±5	±10		±5	±10		±5	±10		mA
	Short Circuit		±15			±15			±15			±15		mA
POWER SUPPLY														
Rated Performance			±15			±15			±15			±15		V
Operating Range		±5		±18	±5		±18	±5		±18	±5		±18	V
Quiescent Current			3.0	3.5		3.0	3.5		3.0	3.5		3.0	3.5	mA
Transistor Count	# of Transistors		62			62			62			62		

NOTES

[1]Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[2]Bias current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperature, the current doubles every 10°C.

[3]Gain = –1, R_{LOAD} = 2 kΩ.

[4]Defined as the time required for the amplifier's output to return to normal operation after removal of a 50% overload from the amplifier input.

[5]Defined as the maximum continuous voltage between the inputs such that neither input exceeds ±10 V from ground.

All min and max specifications are guaranteed.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . ±18 V
Internal Power Dissipation[2] (@ T_A = +25°C)
 8-Pin Header Package . . . . 500 mW
 8-Pin Mini-DIP Package . . . . 750 mW
Input Voltage . . . . $\pm V_S$
Output Short Circuit Duration . . . . Indefinite
Differential Input Voltage . . . . $+V_S$ and $-V_S$
Storage Temperature Range (H) . . . . –65°C to +150°C
Storage Temperature Range (N) . . . . –65°C to +125°C
Operating Temperature Range
 AD645J/K . . . . 0°C to +70°C
 AD645A/B/C . . . . –40°C to +85°C
 AD645S . . . . –55°C to +125°C
Lead Temperature Range
 (Soldering 60 sec) . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Thermal Characteristics:
8-Pin Plastic Mini-DIP Package: θ_{JA} = 100°C/Watt
8-Pin Header Package: θ_{JA} = 200°C/Watt

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD645 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



ORDERING GUIDE

Model[1]	Temperature Range	Package Option[2]
AD645JN	0°C to +70°C	N-8
AD645KN	0°C to +70°C	N-8
AD645AH	–40°C to +85°C	H-08A
AD645BH	–40°C to +85°C	H-08A
AD645CH	–40°C to +85°C	H-08A
AD645SH/883B	–55°C to +125°C	H-08A

NOTES
[1]Chips are also available.
[2]N = Plastic Mini-DIP; H = Metal Can.

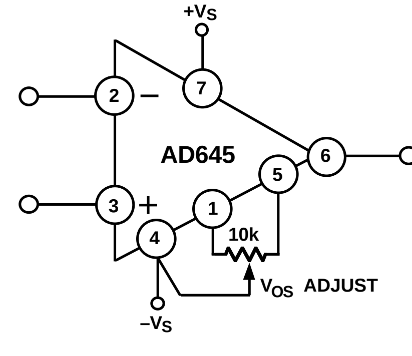
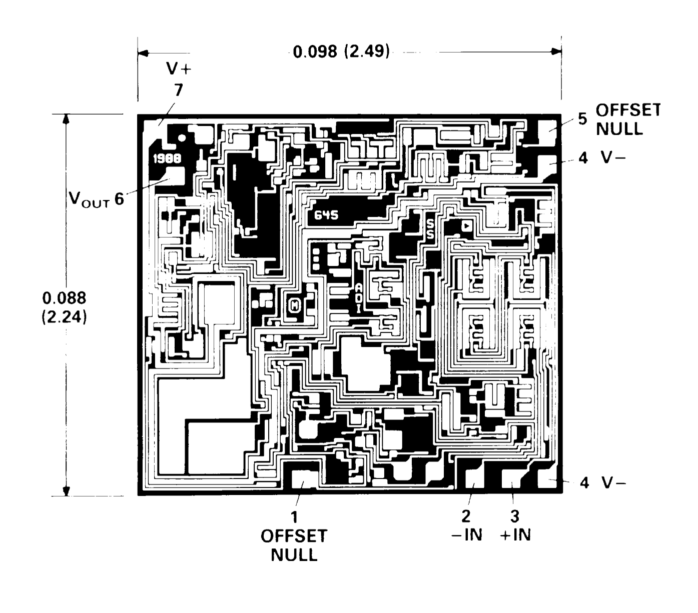
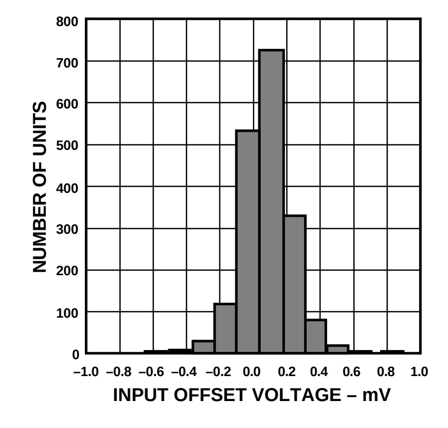


Figure 3. AD645 Offset Null Configuration

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.





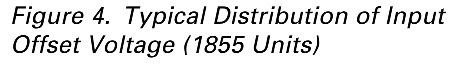

Figure 4. Typical Distribution of Input Offset Voltage (1855 Units)

Figure 5. Typical Distribution of Input Bias Current (576 Units)

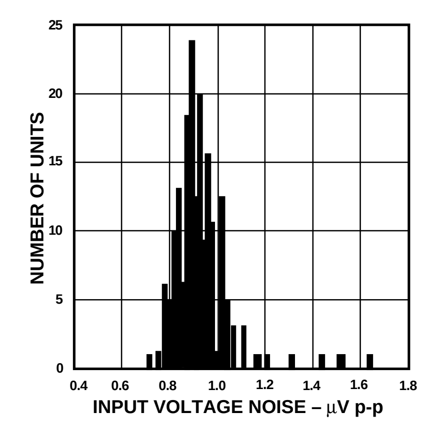


Figure 6. Typical Distribution of 0.1 Hz to 10 Hz Voltage Noise (202 Units)

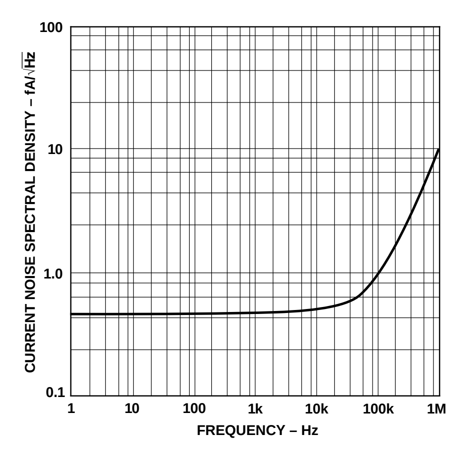


Figure 7. Current Noise Spectral Density vs. Frequency

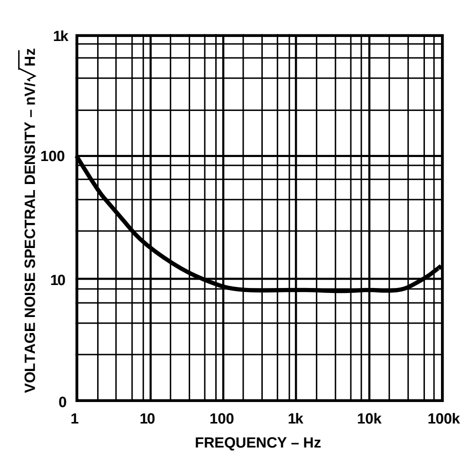


Figure 8. Voltage Noise Spectral Density vs. Frequency

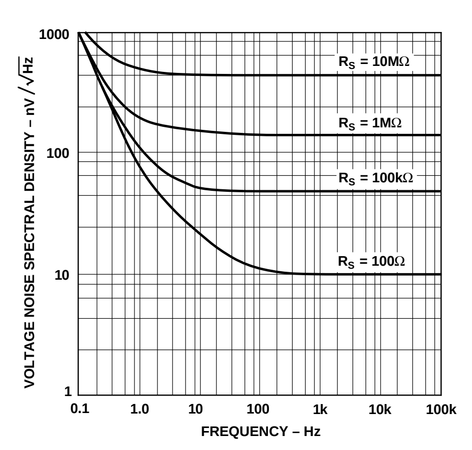


Figure 9. Voltage Noise Spectral Density vs. Frequency for Various Source Resistances

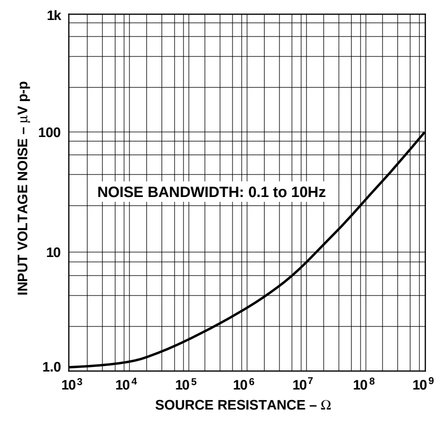


Figure 10. Input Voltage Noise vs. Source Resistance

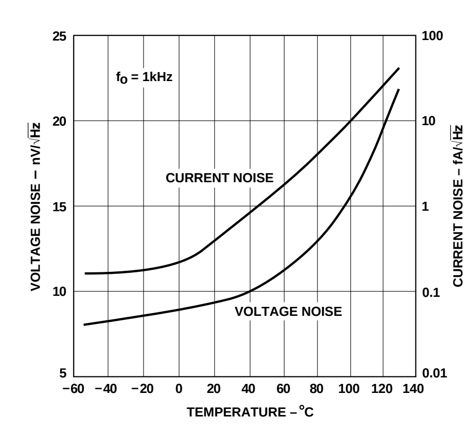


Figure 11. Voltage and Current Noise Spectral Density vs. Temperature

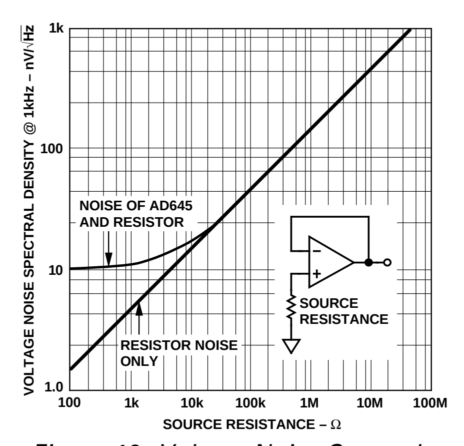


Figure 12. Voltage Noise Spectral Density @ 1 kHz vs. Source Resistance

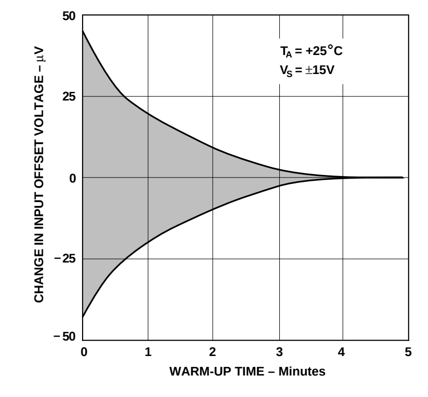


Figure 13. Change in Input Offset Voltage vs. Warmup Time

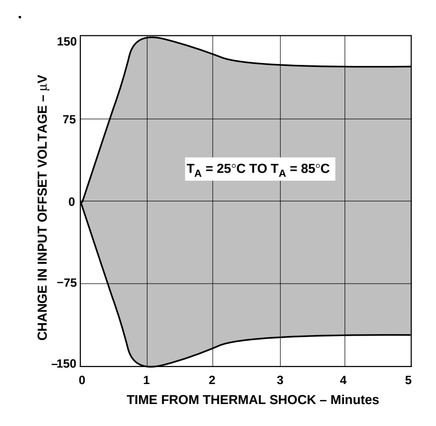


Figure 14. Change in Input Offset Voltage vs. Time from Thermal Shock

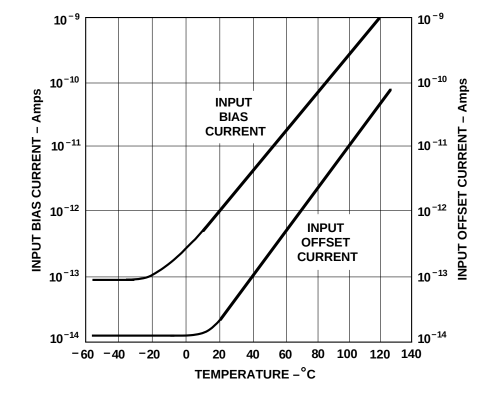


Figure 15. Input Bias and Offset Currents vs. Temperature

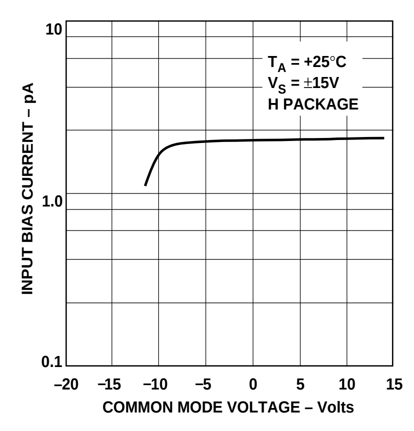


Figure 16. Input Bias Current vs. Common-Mode Voltage

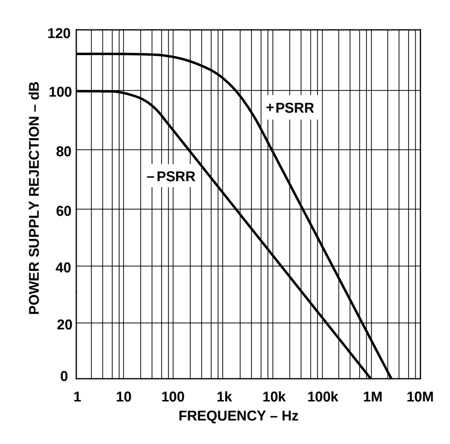


Figure 17. Power Supply Rejection vs. Frequency

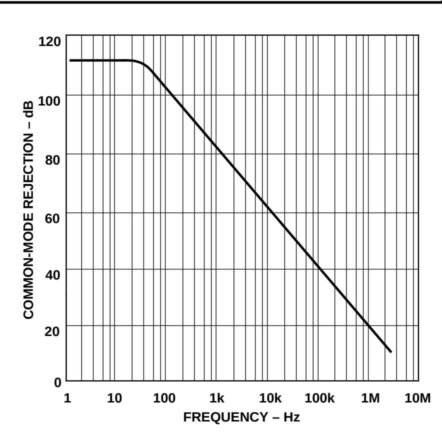


Figure 18. Common-Mode Rejection vs. Frequency

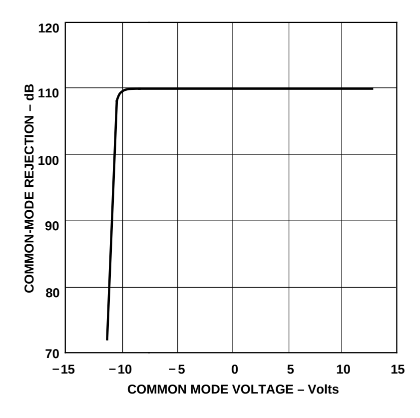


Figure 19. Common-Mode Rejection vs. Input Common-Mode Voltage

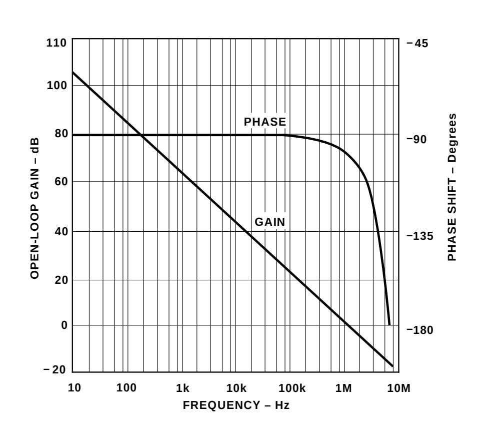


Figure 20. Open-Loop Gain and Phase Shift vs. Frequency

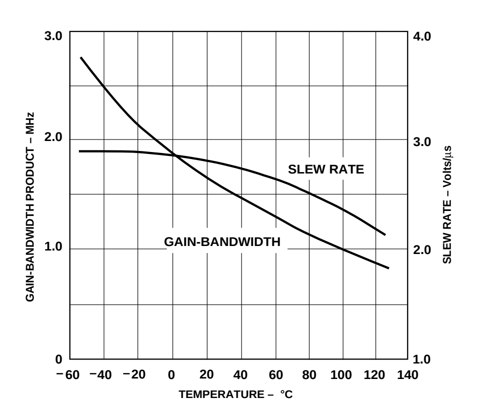


Figure 21. Gain-Bandwidth Product and Slew Rate vs. Temperature

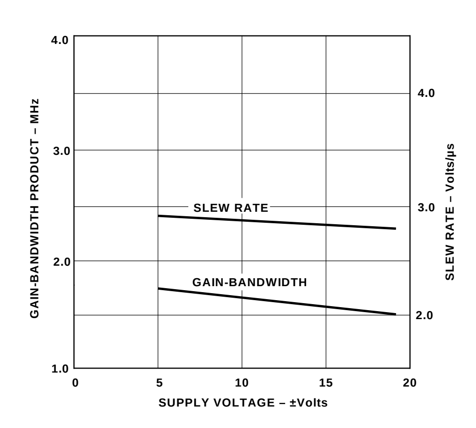


Figure 22. Gain-Bandwidth and Slew Rate vs. Supply Voltage

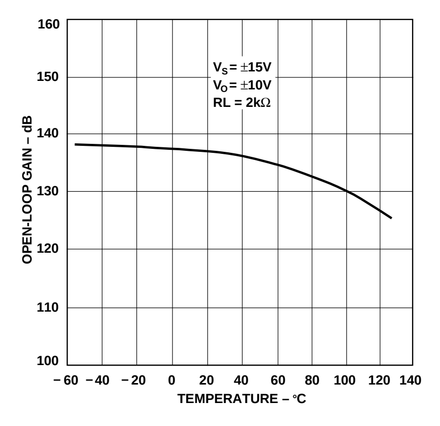


Figure 23. Open-Loop Gain vs. Temperature

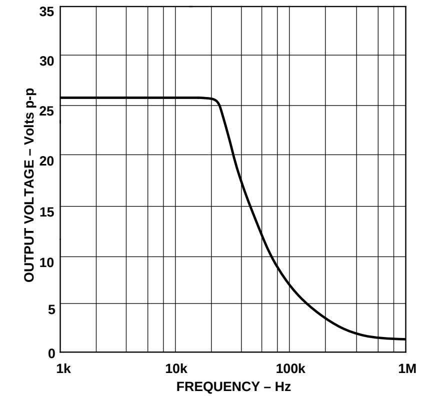


Figure 24. Large Signal Frequency Response

AD645–Typical Characteristics

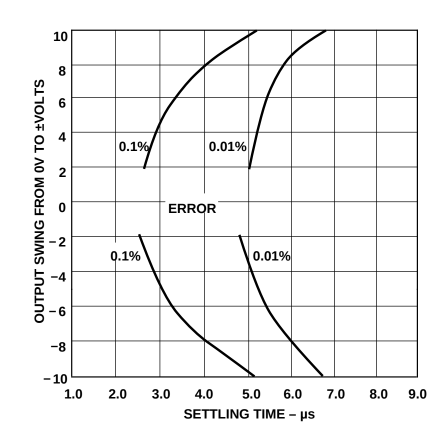


Figure 25. Output Swing and Error vs. Settling Time

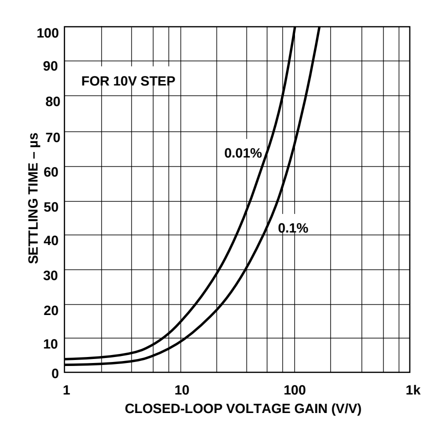


Figure 26. Settling Time vs. Closed-Loop Voltage Gain

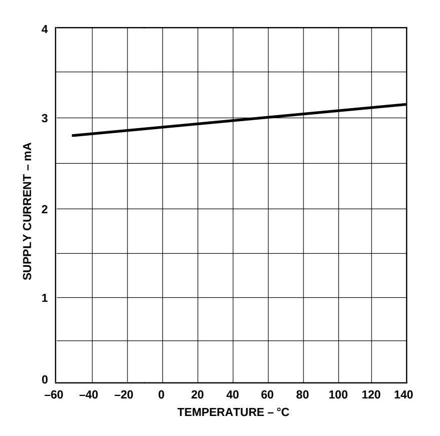


Figure 27. Supply Current vs. Temperature

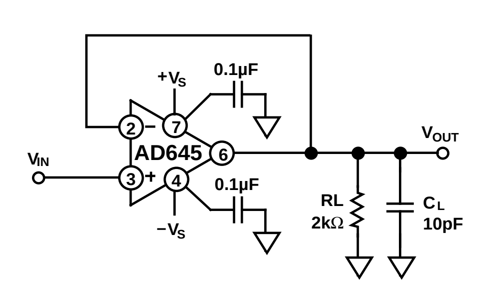


Figure 28a. Unity-Gain Follower

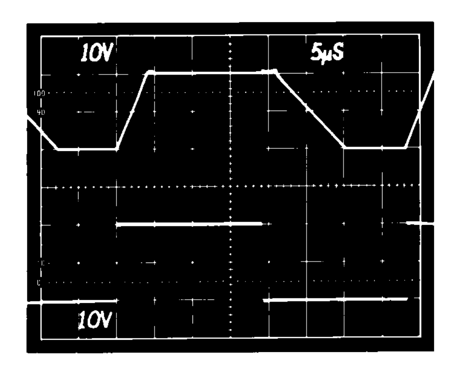


Figure 28b. Unity-Gain Follower Large Signal Pulse Response

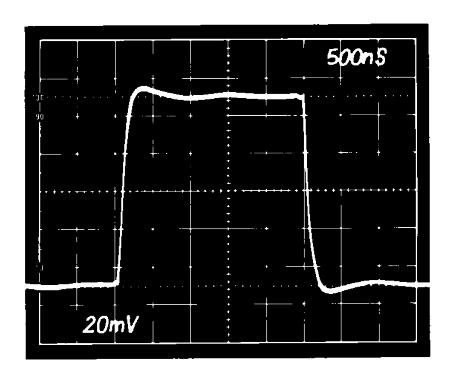


Figure 28c. Unity-Gain Follower Small Signal Pulse Response

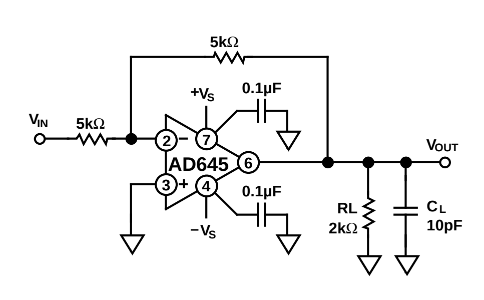


Figure 29a. Unity-Gain Inverter

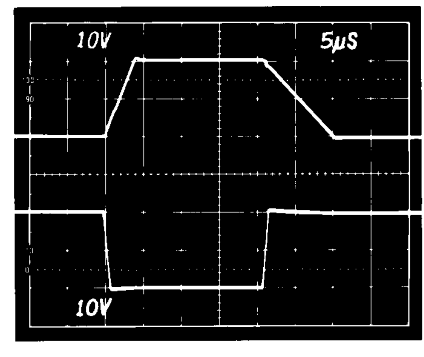


Figure 29b. Unity-Gain Inverter Large Signal Pulse Response

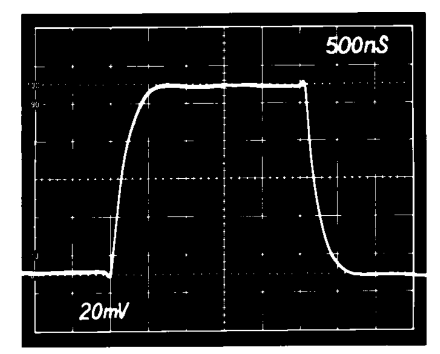


Figure 29c. Unity-Gain Inverter Small Signal Pulse Response

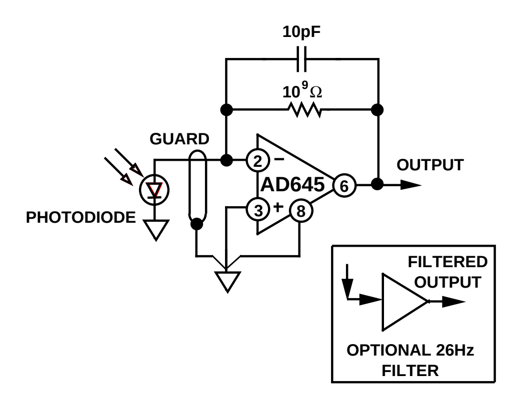


Figure 30. The AD645 Used as a Sensitive Preamplifier

Preamplifier Applications

The low input current and offset voltage levels of the AD645 together with its low voltage noise make this amplifier an excellent choice for preamplifiers used in sensitive photodiode applications. In a typical preamp circuit, shown in Figure 30, the output of the amplifier is equal to:

$$V_{OUT} = I_D\ (Rf) = Rp\ (P)\ Rf$$

where:

I_D = photodiode signal current (Amps)

Rp = photodiode sensitivity (Amp/Watt)

Rf = the value of the feedback resistor, in ohms.

P = light power incident to photodiode surface, in watts.

An equivalent model for a photodiode and its dc error sources is shown in Figure 31. The amplifier's input current, I_B, will contribute an output voltage error which will be proportional to the value of the feedback resistor. The offset voltage error, V_{OS}, will cause a "dark" current error due to the photodiode's finite shunt resistance, Rd. The resulting output voltage error, V_E, is equal to:

$$V_E = (1 + Rf/Rd)\ V_{OS} + Rf\ I_B$$

A shunt resistance on the order of 10^9 ohms is typical for a small photodiode. Resistance Rd is a junction resistance which will typically drop by a factor of two for every 10°C rise in temperature. In the AD645, both the offset voltage and drift are low, this helps minimize these errors.

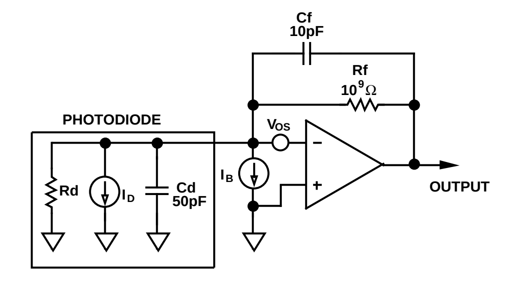


Figure 31. A Photodiode Model Showing DC Error Sources

Minimizing Noise Contributions

The noise level limits the resolution obtainable from any preamplifier. The total output voltage noise divided by the feedback resistance of the op amp defines the minimum detectable signal current. The minimum detectable current divided by the photodiode sensitivity is the minimum detectable light power.

Sources of noise in a typical preamp are shown in Figure 32. The total noise contribution is defined as:

$$\overline{V_{OUT}} = \sqrt{\left(\overline{i_n}^2 + \overline{i_f}^2 + \overline{i_s}^2\right)\left(\frac{Rf}{1+s\,(Cf)\,Rf}\right)^2 + \left(\overline{en}^2\right)\left(1+\frac{Rf}{Rd}\left(\frac{1+s\,(Cd)\,Rd}{1+s\,(Cf)\,Rf}\right)\right)^2}$$

Figure 33, a spectral density versus frequency plot of each source's noise contribution, shows that the bandwidth of the amplifier's input voltage noise contribution is much greater than its signal bandwidth. In addition, capacitance at the summing junction results in a "peaking" of noise gain in this configuration. This effect can be substantial when large photodiodes with large shunt capacitances are used. Capacitor Cf sets the signal bandwidth and also limits the peak in the noise gain. Each source's rms or root-sum-square contribution to noise is obtained by integrating the sum of the squares of all the noise sources and then by obtaining the square root of this sum. Minimizing the total area under these curves will optimize the preamplifier's overall noise performance.

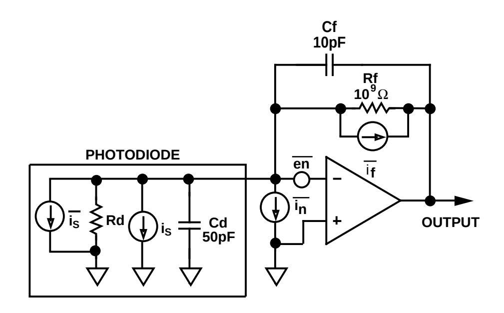


Figure 32. Noise Contributions of Various Sources

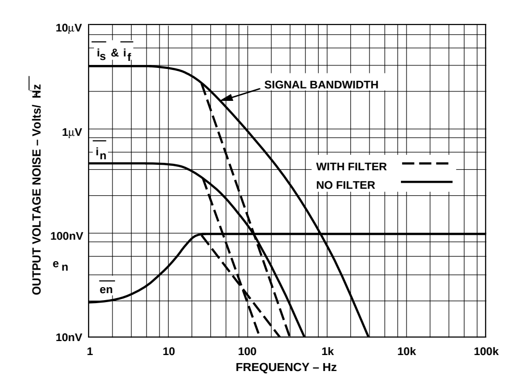


Figure 33. Voltage Noise Spectral Density of the Circuit of Figure 32 With and Without an Output Filter

An output filter with a passband close to that of the signal can greatly improve the preamplifier's signal to noise ratio. The photodiode preamplifier shown in Figure 32—without a bandpass filter—has a total output noise of 50 µV rms. Using a 26 Hz single pole output filter, the total output noise drops to 23 µV rms, a factor of 2 improvement with no loss in signal bandwidth.

Using a "T" Network

A "T" network, shown in Figure 34, can be used to boost the effective transimpedance of an I to V converter, for a given feedback resistor value. Unfortunately, amplifier noise and offset voltage contributions are also amplified by the "T" network gain. A low noise, low offset voltage amplifier, such as the AD645, is needed for this type of application.

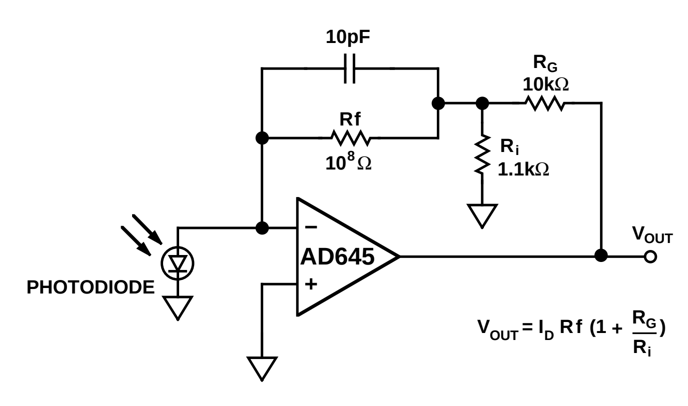


Figure 34. A Photodiode Preamp Employing a "T" Network for Added Gain

A pH Probe Buffer Amplifier

A typical pH probe requires a buffer amplifier to isolate its 10^6 to $10^9\ \Omega$ source resistance from external circuitry. Just such an amplifier is shown in Figure 35. The low input current of the AD645 allows the voltage error produced by the bias current and electrode resistance to be minimal. The use of guarding, shielding, high insulation resistance standoffs, and other such standard methods used to minimize leakage are all needed to maintain the accuracy of this circuit.

The slope of the pH probe transfer function, 50 mV per pH unit at room temperature, has a +3300 ppm/°C temperature coefficient. The buffer of Figure 35 provides an output voltage equal to 1 volt/pH unit. Temperature compensation is provided by resistor RT which is a special temperature compensation resistor, part number Q81, 1 kΩ, 1%, +3500 ppm/°C, available from Tel Labs Inc.

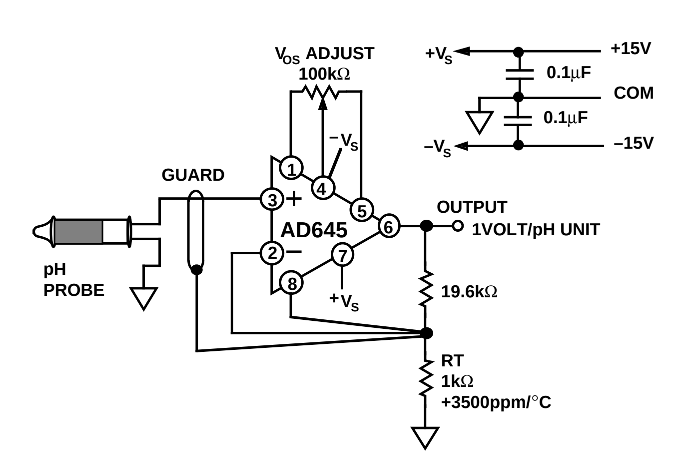


Figure 35. A pH Probe Amplifier

Circuit Board Notes

The AD645 is designed for through hole mount into PC boards. Maintaining picoampere level resolution in that environment requires a lot of care. Since both the printed circuit board and the amplifier's package have a finite resistance, the voltage difference between the amplifier's input pin and other pins (or traces on the PC board) will cause parasitic currents to flow into (or out of) the signal path. These currents can easily exceed the 1.5 pA input current level of the AD645 unless special precautions are taken. Two successful methods for minimizing leakage are: guarding the AD645's input lines and maintaining adequate insulation resistance.

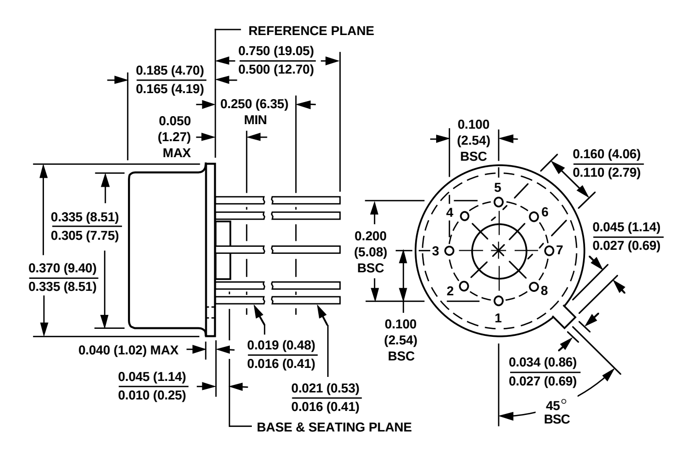
Guarding the input lines by completely surrounding them with a metal conductor biased near the input lines' potential has two major benefits. First, parasitic leakage from the signal line is reduced, since the voltage between the input line and the guard is very low. Second, stray capacitance at the input terminal is minimized which in turn increases signal bandwidth. In the header or can package, the case of the AD645 is connected to Pin 8 so that it may be tied to the input potential (when operating as a follower) or tied to ground (when operating as an inverter). The AD645's positive input (Pin 3) is located next to the negative supply voltage pin (Pin 4). The negative input (Pin 2) is next to the balance adjust pin (Pin 1) which is biased at a potential close to that of the negative supply voltage. Note that any guard traces should be placed on *both* sides of the board. In addition, the input trace should be guarded along both of its edges, along its entire length.

Contaminants such as solder flux, on the board's surface and on the amplifier's package, can greatly reduce the insulation resistance and also increase the sensitivity to atmospheric humidity. Both the package and the board must be kept clean and dry. An effective cleaning procedure is to: first, swab the surface with high grade isopropyl alcohol, then rinse it with deionized water, and finally, bake it at 80°C for 1 hour. Note that if either polystyrene or polypropylene capacitors are used on the printed circuit board that a baking temperature of 70°C is safer, since both of these plastic compounds begin to melt at approximately +85°C.

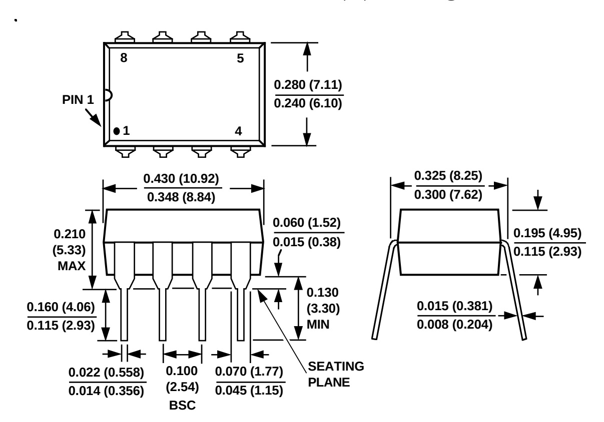
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

TO-99 Header (H) Package



Plastic Mini-DIP (N) Package



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